



PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2DC		SERIAL NUMBER 09/545,648
	APPLICANT(S) FARMWALD ET AL.		
	FILING DATE April 10, 2000	GROUP ART UNIT 2781	

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
DA	4,445,204	04/24/84	Nishiguchi	—	—	
DA	4,821,226	04/11/89	Christopher et al.	—	—	
DA	4,882,712	11/21/89	Ohno et. al.	—	—	
DA	4,951,251	08/21/90	Yamaguchi et al.	—	—	
DA	4,928,265	5 12/29/91 22 Higuchi et al.	Higuchi et al.	—	—	
DA	5,107,465	04/21/92	Fung et al.	—	—	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

DA 1	T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul., Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
✓ DA 2	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983)
DA 3	A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)

EXAMINER <i>Glen Aune</i>	DATE CONSIDERED <i>9/6/2000</i>
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MS	5,206,833	04/27/93	Lee	—	—	
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GA	5,018,111	05/21/91	Madland	—	—	
GA	4,845,664	07/04/89	Aichelmann, Jr. et al.	—	—	
GA	4,734,880	03/29/88	Collins	—	—	

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✓ GA 4	D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
✓ GA 5	T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)
✓ GA 6	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87)
✓ GA 7	F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987
✓ GA 8	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
✓ GA 9	K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
✓ GA 10	F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)
✓ GA 11	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference
✓ GA 12	D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)

EXAMINER Glen June	DATE CONSIDERED 9/6/2000
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J 13	S. Watanabe et. al., "AN Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982) ✓
J 14	K. Numata et. al. " New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989) ✓
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J 16	J. Sonntag et al. "A Monolithic CMOS 10MHz DPLL for Burst-Mode Data Retiming", IEEE International Solid State Circuits Conference (ISSCC) February 16, 1990

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JM	4,860,198	08/22/89	Takenaka	—	—	
JM	3,969,706	07/13/76	Proebsting et al.	—	—	
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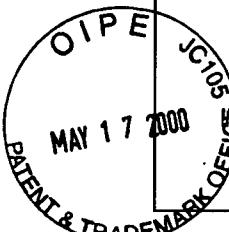
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
JM	0 276 871 ✓	03/08/88	DEFR GBTI EPX	—	—	

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✓ JM 17	M. Horowitz et. al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with On-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987) ✓ .
✓ JM 18	R. L. Schmidt, "A memory Control Chip for Formatting Data into Blocks Suitable for Video Coding Applications", IEEE Transactions on Circuits And Systems, vol. 36 No. 10, pp. 1275-1280 (Oct 1989) ✓ .
✓ JM 19	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. SC-18 No. 5, pp. 561-567 (Oct. 1983) ✓ .
✓ JM 20	A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989) ✓ .

EXAMINER	DATE CONSIDERED
Glenne Anne	9/6/2003

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DA	4,685,088	08/04/87	Iannucci	—	—	
DA	4,509,142	04/02/85	Childers	—	—	
DA	5,051,889	09/24/91	Fung et al.	—	—	
DA	5,361,277	11/01/94	Grover	—	—	
DA	4,954,987	09/04/90	Auvinen et al.	—	—	
DA	4,570,220	02/11/86	Tetrick et al.	( )	—	
DA	4,247,817	01/27/81	Heller	—	—	
DA	4,519,034	05/21/85	Smith et al.	—	—	
DA	3,691,534	09/12/72	Varadi et al.	—	—	
DA	4,920,486	04/24/90	Nielsen	—	—	
DA	4,263,650	04/21/81	Bennett et al.	—	—	

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DA	0 276 871	03/08/88	DE FR GB IT EPX	—	—	

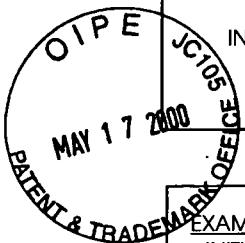
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✓ DA 22	J. Peterson, "System-Level Concerns Set Performance Gains", High Performance Systems, pp. 71-77 (Sept. 89) ✓
✓ DA 23	N. Margulis, "Single Chip CPU Eases Single Chip System Design", High Performance Systems, pp. 34-44 (Sept. 89) ✓
✓ DA 24	F.Nart, "Multiple Chips Speed CPU Subsystems", High Performance Systems, pp. 46-55 (Sept. 89) ✓
✓ DA 25	D.T. Wong, "An 11-ns 8Kx18 CMOS Static RAM with 0.5-um Devices", IEEE Journal of Solid State Circuits, vol. 23, No. 5, pp. 1095-1103 (Oct. 1988) ✓
✓ DA 26	A. Agarwal et al., "An Evaluation of Directory Schemes for Cache Coherence", IEEE, pp. 280-289, 1988 ✓

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MA 28	D. Hawley, "Superfast Bus Supports Sophisticated Transactions", High Performance Systems, pp. 90-94 (Sept. 89)
MA 29	M. Bazes, A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. SC-18, No. 2, pp. 164-172 (April 1983)
DA 30	D. Wendell et al., "A 3.5ns Self Timed SRAM", IEEE 1990 Symposium on VLSI Circuits pp. 49-50
GA 31	J. Chun et al., "A pipelined 650 MHz GaAs 8K ROM with Translation Logic" IEEE 1990 GaAs IC Symposium, pp 139-142
MA 32	A. L. Yuen, "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Oct. 1989)

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Glenn Aune	9/6/2002

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Sheet 1 of 1

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JA	4,630,193	Dec. 16, 1986	Kris	—	—	
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✓ JA 33	European Search Report for EPO Patent Application No. 00 10 0018
✓ JA 34	European Search Report for EPO Patent Application No. 00 10 822

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<i>PA</i>	S56-82961	July 7, 1981	Japan	—	—	YES
<i>PA</i>	S57-14922	Jan. 26, 1982	Japan	—	—	YES
<i>PA</i>	Sho 60-80193	May 8, 1983	Japan	—	—	YES
<i>PA</i>	Sho 60-55459	Mar. 30, 1985	Japan	—	—	YES
<i>PA</i>	S61-72350	April 14, 1986	Japan	—	—	YES
<i>PA</i>	S63-142445	June 14, 1988	Japan	—	—	YES
<i>PA</i>	B63-46864	Sept. 19, 1988	Japan	—	—	YES
<i>PA</i>	S64-29951	Jan. 31, 1989	Japan	—	—	YES

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<i>PA</i>	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
<i>PA</i>	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

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MM	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)
AB	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
MM	JEDEC Standard No. 21C

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